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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,571	DOCKSER, KENNETH	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2009 and 02 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,7-10 and 21-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-10 and 21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 7-10, and 21-34 have been considered. Claims 2-3, 5-6, and 11-20 have been canceled.

2. In view of the Appeal Brief filed on 29 April 2009 and 02 July 2009, PROSECUTION IS HEREBY REOPENED. A new rejection is set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

4. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Papers Submitted

5. It is hereby acknowledged that the following papers have been received and placed of record in the file: Appeal Brief as filed 29 April 2009 and Appeal Brief as filed 02 July 2009.

Response to Arguments

6. Applicant's arguments, see Appeal Briefs, filed 29 April 2009 ad 02 July 2009, with respect to the rejection(s) of claim(s) have been fully considered and are persuasive. Therefore,

the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the following.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1, 4, 7-10, and 21-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The independent claims use the wording "substantially", however there is no language in the claim or specification regarding the exact scope of this terminology.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 4, 7-8, and 21-34 are rejected under 35 U.S.C. 102(b) as being taught by Park et al., U.S. Patent Number 5,881,307 (herein referred to as Park) and Nguyen, U.S. Patent Number 6,058,465 (herein referred to as Nguyen), which is incorporated by reference in Park in column 3, lines 34-38..

11. Referring to claim 1, Park has taught a microprocessor, comprising:

a. a vector unit to execute a vector instruction to perform a first operation on a first set of three operands and a second operation on a second set of three operands

(Park Figure 1, elements 140 and 142), said vector unit configured with three inputs, one for each of the three operands, which are received at the vector unit at substantially a same time (Park column 3, line 7 to column 4, line 44);

b. a vector register file having a primary register file and a secondary register file (Park Figure 1, elements 130 and 132), each having a first register, a second register and a third register with the operands provided therein (Park column 3, line 7 to column 4, line 44);

c. wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file (Park column 3, line 7 to column 4, line 44); and

a. wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (Park column 3, line 7 to column 4, line 44), wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs (Park column 3, line 7 to column 4, line 44; Figure 1, element 135).

12. Referring to claim 4, Park has taught the microprocessor of claim 1, wherein the vector unit includes a 3-input primary unit and a 3-input secondary unit, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands (Park column 3, line 7 to column 4, line 44; Figure 1, elements 140 and 142).

2. Referring to claim 7, Park has taught the microprocessor of claim 1, wherein the first and second operations use at least one operand from the primary register file and at least one operand from the secondary register file (Park column 3, line 7 to column 4, line 44).

13. Referring to claim 8, Park has taught the microprocessor of claim 1, wherein the first and second sets of operands include at least one common operand (Park column 3, line 7 to column 4, line 44).

14. Referring to claim 21, Park has taught the microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (Park column 3, line 7 to column 4, line 44; Figure 1, element 135).

15. Referring to claim 22, Park and Nguyen has taught the microprocessor of claim 4, wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product (Nguyen Figure 4; Figure 6A).

16. Referring to claim 23, Park and Nguyen has taught the microprocessor of claim 22, wherein the first and second sets of operands comprise first and second sets of floating point formatted operands (Nguyen Abstract).

17. Referring to claim 24, Park has taught the microprocessor of claim 1, wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register (Park column 3, line 7 to column 4, line 44).

18. Referring to claim 25, Park has taught a vector unit to process a vector instruction having an opcode and first, second, and third register fields, comprising:

a. a register file including a primary register file having a set of primary registers and a secondary register file having a set of secondary registers (Park Figure 1, elements 130 and 132), wherein each register field identifies a register in the primary register file and a corresponding register in the secondary register file, wherein the set of primary registers and set of secondary registers each have a first register, a second register and a third register with operands provided therein (Park column 3, line 7 to column 4, line 44);

b. primary and secondary calculating units (Park figure 1, elements 140 and 142), wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes first, second, and third inputs

to receive, respectively, first, second, and third operands of a second set of operands (Park column 3, line 7 to column 4, line 44);

c. wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register, wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs (Park column 3, line 7 to column 4, line 44; Figure 1, element 135);

d. wherein the three operands are received at the vector unit from the register files at substantially a same time (Park column 3, line 7 to column 4, line 44); and

e. multiplexing circuitry (Park Figure 1, elements 135 and 160) controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields (Park column 3, line 7 to column 4, line 44).

19. Referring to claim 26, Park has taught the vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select:

a. the first operand in the first set of operands from either the first primary or the first secondary registers (Park column 3, line 7 to column 4, line 44);

b. the second operand in the first set of operands from either the second primary or the second secondary registers (Park column 3, line 7 to column 4, line 44); and

c. the third operand in the first set of operands from either the third primary or the third secondary registers (Park column 3, line 7 to column 4, line 44);

d. the first operand in the second set of operands from either the first primary or the first secondary registers (Park column 3, line 7 to column 4, line 44),

e. the second operand in the second set of operands from either the second primary or the second secondary registers (Park column 3, line 7 to column 4, line 44); and

f. the third operand in the second set of operands from either the third primary or the third secondary registers (Park column 3, line 7 to column 4, line 44).

20. Referring to claim 27, Park has taught the vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands (Park column 3, line 7 to column 4, line 44).

21. Referring to claim 28, Park has taught the vector unit of claim 27, wherein the first operation differs from the second operation (Park column 3, line 7 to column 4, line 44).

22. Referring to claim 29, Park and Nguyen has taught the vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products (Nguyen Figure 4; Figure 6A).

23. Referring to claim 30, Park and Nguyen has taught the vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands (Nguyen Abstract).

24. Referring to claim 31, Park has taught a microprocessor including:

a. an execution unit enabled to execute an asymmetric instruction (Park Figure 1, elements 140 and 142), wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode) (Park column 3, line 7 to column 4, line 44);

b. a register file accessible by the execution unit and having a rank of two (Park Figure 1, elements 130 and 132) including a primary register file and a secondary register file wherein a value in an operand register field identifies a register in the primary register file and a corresponding register in the secondary register file, wherein the set of primary registers and set of secondary registers each have a first register, a second register and a third register with operands provided therein (Park column 3, line 7 to column 4, line 44);

c. wherein the execution unit is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode (Park column 3, line 7 to column 4, line 44);

d. wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand

selected from the third primary register or the third secondary register, wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs (Park column 3, line 7 to column 4, line 44); and

e. wherein the three operands are received from the register files at substantially a same time (Park column 3, line 7 to column 4, line 44).

25. Referring to claim 32, Park has taught the microprocessor of claim 31, wherein at least one condition selected from a group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true (Park column 3, line 7 to column 4, line 44).

26. Referring to claim 33, Park has taught the microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field (Park column 3, line 7 to column 4, line 44).

27. Referring to claim 34, Park has taught the microprocessor of claim 31, including multiplexing circuitry controlled by the opcode (Park Figure 1, elements 135 and 160) to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first

secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field (Park column 3, line 7 to column 4, line 44).

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Nguyen as applied to claim 1 above, and further in view of Official Notice.

30. Referring to claim 9, Park and Nguyen has not taught the microprocessor of claim 1, wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file. Official Notice is taken. A person of ordinary skill in the art at the time the invention was made would have recognized that performing operations on complex numbers increases flexibility of the processor.

31. Referring to claim 10, Park and Nguyen in view of Official Notice has taught the microprocessor of claim 9, wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in

which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (Nguyen Figure 4; Figure 6A).

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Wang et al., U.S. Patent Number 5,187,796, has taught parallel processing of three operands in a processor and the operands are all stored in register files.

b. Cho et al., U.S. Patent Number 5,922,066, is related to the references used in the rejection above.

c. Moreno et al., U.S. Patent Number 6,915,411, has taught selecting operands from register files for SIMD operations.

d. Dworkin et al., U.S. Patent Number 7,142,669, has taught selecting 3 operands from register files.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183
12 October 2009

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Primary Examiner, Art Unit 2183